

JAPANESE PATENT OFFICE – Patent Abstracts of Japan

Publication Number: 09017832 A

Date of Publication: 1997.01.17

Int.Class: H01L 21/66

Date of Filing: 1995.06.27

Applicant: MATSUSHITA ELECTRIC IND
CO LTD

Inventor: HIRANO HIROSHIGE
TANIGUCHI TAKASHI
SEMICONDUCTOR DEVICE

Abstract

PURPOSE: To execute the burn in of a plurality of semiconductor devices at the same time in wafer condition.

CONSTITUTION: Power voltage wirings 205 and 207 capable of external connection for wafer burn in and earth voltage wirings 206 and 208 are arranged in lattice shape so that they may pass the interior of each of a plurality of semiconductor devices 204 made on one sheet of a wafer. Each semiconductor device 204 has an inner power voltage pad 219 and an inner earth voltage pad 220 each given power voltage for quality inspection and earth voltage, and an inner power voltage wiring 213 connected to the inner power voltage pad 219, an inner earth voltage wiring 214 connected to the inner earth voltage pad 220, and four pieces of n-channel type MOS transistors 223 and 226. In case that the semiconductor device 204 is an article of good quality, the four pieces of transistors 223-226 electrically connect the inner wirings 213 and 214 to the wirings 205 and 206 for wafer burn in.

COPYRIGHT: (C)1997,JPO

